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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,702	07/24/2003	Franciscus Maria Leonardus van der Goes	1875.2820002	1071

26111 7590 08/01/2006

STERNE, KESSLER, GOLDSTEIN & FOX PLLC
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
NGUYEN, LINH V	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 08/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,702	VAN DER GOES ET AL.	
	Examiner	Art Unit	
	Linh V. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 –20, 32, and 35 – 40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 –20, 32, and 35 – 40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in communication is in response to preliminary 10/29/04. Claims 21 – 31 and 34 have been canceled. Claims 35 – 40 have been added. Claims 1, 6 – 8, 11 – 20 and 32 – 33 have been amended. Claims 1 – 20, 32, 33, and 35 – 40 are pending on this application.

Double Patenting

2. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

3. Claim 33 is rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 31 of prior U.S. Patent No. 6,653,996. This is a double patenting rejection.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29

USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1 –20, 32, and 35 – 40 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1 – 30 and 32 of U.S. Patent No. 6,653,966. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1 – 30 and 32 of U.S. Patent No. 6,653,966 disclosed every limitation of claims 1 –20, 32, and 35 – 40.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1 – 20, and 35 - 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Brandt U.S patent No. 6,1043,321.

Regarding claim 1, Fig. 1 of Brandt discloses an analog to digital converter (ADC) comprising: a first amplifier (10; See Fig. 10 for disclosed a detailed circuit of 10) tracking an input voltage with its output; a coarse ADC amplifier (12; See Fig. 5 for

disclosing a detailed circuit of 12 having an amplifier 44A) connected to a coarse capacitor (Fig. 5 [C]) at its input and having a coarse ADC reset switch (Fig. 5[Switches at input of 44]) controlled by a first clock phase (M); a fine ADC amplifier (20; See Fig. 7 for disclosing a detailed circuit of 20 having an amplifier 50) connected to a fine capacitor (Fig. [C]) at its input and having a fine ADC reset switch (Fig. 7[Switches at input of 44]) controlled by a second clock phase (Fig. 7[I]), wherein a set of reference voltages (REF) is selected for use by the fine ADC amplifier (Fig. 7[50]) based on an output of the coarse ADC amplifier (Col. 3 lines 62 – 66), wherein the coarse capacitor (Fig. 5 [C]) is charged to a coarse reference voltage during the first clock phase (Fig. 5[M]) and connected to the first amplifier's output voltage (Fig. 5 [VIN]) during the second clock phase (Fig. 5[I]), and wherein the fine capacitor (Fig. 7[C]) is connected to a fine reference voltage (Fig. [REF]) during the first clock phase (Fig. 7[M]) and charged to first amplifier output voltage (Fig. 7 [VIN]) during the second clock phase (Fig. 7 [I]); and an encoder (Fig. 1 [18, 26]) that converts outputs of the coarse (Fig. 1[12]) and fine ADC amplifier (Fig. 1[20]) to a digital output (Fig. 1[28, 32]).

Regarding claim 2, wherein the coarse ADC reset switch is a field effect transistor (Col. 13 lines 27 – 29 disclosed Pmos and Nmos transistor switches).

Regarding claim 3,Fig. 6 of Brandt further discloses wherein the firs (M) and second (I) phases are non-overlapping.

Regarding claim 4, wherein the fine ADC amplifier includes a plurality of cascaded amplifier stages (Fig. 7 [50, 52]).

Regarding claim 5, Fig. 5 further discloses wherein the coarse ADC amplifier (fig. 5) includes a plurality of cascaded amplifier stages (44 amplifier cascaded with amplifier Latch 46; See Col. 12 lines 25 – 29 for disclosing amplifier stages of the latch circuit 46).

Regarding claim 6, wherein the coarse capacitor (Fig. 5 [C] at inputs of [44]) is connected to the first amplifier output (Fig. 1[10]) on a delayed second phase (Fig. 6 [I] is a delayed second phase with respect to the first phase [M]).

Regarding claim 7, wherein the fine ADC capacitor (Fig. 7 [C] at inputs of [50]) is connected to the first amplifier output (Fig. 1[10]) on a delayed second clock phase (Fig. 6 [I] and to the fine reference voltage (Fig. 7[REF]) during a delayed first clock phase (Fig. 6 [M])

Regarding claim 8, Fig. 1 further including a switch (14A, 14B) that connects an output (VIN) of the first amplifier (10) to the coarse capacitor on the second clock phase (Fig. 6 [I]).

Regarding claim 9, fig. 5 further including a coarse comparator (46A) (See Col. 2 lines 33 – 34) that latches (Latch) the output of the coarse ADC amplifier (44) and outputs it to the encoder (Fig. 1[18]).

Regarding claim 10, Fig. 7 further including a fine comparator (56A) (See Col. 2 lines 33 – 34) that latches (Latch) the output of the fine ADC amplifier (50) and outputs it to the encoder (Fig. 1 [26]).

Regarding claim 11, Fig. 1 of Brandt discloses an analog to digital converter comprising: a track-and-hold (10) amplifier (see Fig. 10) tracking an input voltage

(Vinse); a first plurality amplifiers (Fig. 5 [44A, 44B, 44C]) each connected to a corresponding capacitor (fig. 5[C]) at its input, wherein the amplifiers of the first plurality are reset on a clock phase 1 (fig. 5 [M]) and their corresponding capacitors are connected to an output of the track-and-hold on a clock phase 2 (Fig. 5 [I]) (See Fig. 6); a second plurality of amplifiers (Fig. 7 [50A, 50B]) each connected to a corresponding capacitor (Fig. 7[C])at its input, wherein the amplifiers of the second plurality are reset on the clock phase (Fig. 7[I]) and their corresponding capacitors are charged to the track-and-hold amplifier output voltage (VIN) on the clock (Fig. 7 [I])and wherein a set of reference voltages (Fig. [REF]) is selected based on outputs of the first plurality of amplifiers (Col. 3 lines 62 – 66), for input to the second plurality of amplifiers on the clock phase 1 (Fig. 7 [M]); and an encoder (Fig. 1 [18, 20]) that converts outputs of the first and second plurality of amplifier to a digital output (Fig. 1[28,32]).

Regarding claim 12, Col. 13 lines 27 – 28 further including
FET switches (Fig. 5 [R, M]) that reset the first plurality of amplifier on the clock phase (I).

Regarding claim 13, wherein the clock phase1 (M) and phase 2 (I) are non-overlapping (Fig. 6).

Regarding claim 14, wherein each of the second plurality of amplifiers (fig. 7) includes a plurality of cascaded amplifier stages (50, 52).

Regarding claim 15, Fig. 5 further discloses wherein the coarse ADC amplifier (fig. 5) includes a plurality of cascaded amplifier stages (44 amplifier cascaded with

amplifier Latch 46; See Col. 12 lines 25 – 29 for disclosing amplifier stages of the latch circuit 46).

Regarding claim 16, wherein the capacitors (Fig. 5[C]) of the first plurality of amplifiers (Fig. 5 ([44A, B, C]) are connected to the track-and-hold amplifier (Fig. 1 [10]) output (VIN) on a delayed clock phase 2 (Fig 6 [I]).

Regarding claim 17, wherein the capacitors (fig. 7[C])of the second plurality of amplifiers (fig. 7[50, 52]) are connected to the track-and-hold amplifier (Fig. 1[10]) output (VIN) on a delayed clock phase 2 (Fig. 6 [I]), and to the set of reference voltages on a delayed clock phase 1 (Fig. 6 [M]).

Regarding claim 18, Fig. 1 further including switches (14A, 14B) that connect an output of the track-and-hold (10) to the capacitors of the first plurality of amplifiers (Fig. 5) on the clock phase 2 (Fig. 6[I]).

Regarding claim 19, Fig. 5 further including a first plurality of comparators (46A, B, C, D, E) (See Col. 2 lines 33 – 34) that latch (Latch) the outputs of the first plurality of amplifiers (Fig. 5) and output them to the encoder (Fig. 1 [18]).

Regarding claim 20, Fig. 7 further including a second plurality of comparators (54A, B, C, D, E) (See Col. 2 lines 33 – 34) that latch (Latch) the outputs of the second plurality of amplifiers (Fig. 7 [50a, B]) and output them to the encoder (Fig. 1 [26]).

Regarding claim 35, wherein the first amplifier (Fig. 10) is in a hold-mode (Fig. 11B) during the second clock phase (col. 15 lines 10 – 13)

Regarding claim 36, Fig. 3 further including a switch matrix (24) to select the set of reference voltages (REF) for use by the fine ADC amplifier (20).

Regarding claim 37, wherein the track-and-hold amplifier (Fig. 10) is in a hold-mode (Fig. 11B) on the clock phase 2 (col. 15 lines 10 – 13).

Regarding claim 38, Fig. 3 further including a switch matrix (24) to select the set of reference voltages (REF) based on the outputs of the first plurality of amplifiers (See Fig. 1).

Prior Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Contact Information

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Rexford Barnie can be reached at (571) 272-7492. The fax phone numbers for the organization where this application or proceeding is assigned are (571-273-8300) for regular communications and (571-273-8300) for After Final communications.

7/14/06

Linh Van Nguyen

Art Unit 2819

LINH NGUYEN
PRIMARY EXAMINER